

Refine Search

Search Results -

Terms	Documents
L2 and trench	7

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 IBM Technical Disclosure Bulletins

Search:

L3

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Recall Text

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DATE: Sunday, September 05, 2004 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L3</u>	L2 and trench	7	<u>L3</u>
<u>L2</u>	L1 and (polysilicon near2 fill)	7	<u>L2</u>
<u>L1</u>	jfet and mosfet	1343	<u>L1</u>

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Hit List

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
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Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 6707095 B1

L3: Entry 1 of 7

File: USPT

Mar 16, 2004

US-PAT-NO: 6707095

DOCUMENT-IDENTIFIER: US 6707095 B1

TITLE: Structure and method for improved vertical MOSFET DRAM cell-to-cell isolation

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 2. Document ID: US 6576516 B1

L3: Entry 2 of 7

File: USPT

Jun 10, 2003

US-PAT-NO: 6576516

DOCUMENT-IDENTIFIER: US 6576516 B1

TITLE: High voltage power MOSFET having a voltage sustaining region that includes doped columns formed by trench etching and diffusion from regions of oppositely doped polysilicon

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 3. Document ID: US 6441422 B1

L3: Entry 3 of 7

File: USPT

Aug 27, 2002

US-PAT-NO: 6441422

DOCUMENT-IDENTIFIER: US 6441422 B1

TITLE: Structure and method for ultra-scalable hybrid DRAM cell with contacted P-well

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 4. Document ID: US 6291298 B1

L3: Entry 4 of 7

File: USPT

Sep 18, 2001

US-PAT-NO: 6291298

DOCUMENT-IDENTIFIER: US 6291298 B1

TITLE: Process of manufacturing Trench gate semiconductor device having gate oxide layer with multiple thicknesses

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw. De
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☐ 5. Document ID: US 6284593 B1

L3: Entry 5 of 7

File: USPT

Sep 4, 2001

US-PAT-NO: 6284593

DOCUMENT-IDENTIFIER: US 6284593 B1

TITLE: Method for shallow trench isolated, contacted well, vertical MOSFET DRAM

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw. De
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☐ 6. Document ID: US 6121089 A

L3: Entry 6 of 7

File: USPT

Sep 19, 2000

US-PAT-NO: 6121089

DOCUMENT-IDENTIFIER: US 6121089 A

TITLE: Methods of forming power semiconductor devices having merged split-well body regions therein

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw. De
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☐ 7. Document ID: US 6078090 A

L3: Entry 7 of 7

File: USPT

Jun 20, 2000

US-PAT-NO: 6078090

DOCUMENT-IDENTIFIER: US 6078090 A

TITLE: Trench-gated Schottky diode with integral clamping diode

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw. De
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Generate Collection

Print

Fwd Refs

Bkwd Refs

Generate OACS

Terms

Documents

L2 and trench

7

Display Format: **Change Format**

[Previous Page](#)

[Next Page](#)

[Go to Doc#](#)